DATA SHEET

74ABT16260/74ABTH16260

12-bit to 24-bit multiplexed D-type latches (3-State)

Product specification
Supersedes data of 1996 Nov 20
IC23 Data Handbook

1998 Feb 10

Philips
Semiconductors

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12-bit to 24-bit multiplexed D-type latches (3-State)

74ABT16260
74ABTH16260

FEATURES

- ESD protection exceeds 2000V per Mil-Std-883C, Method 3015; exceeds 200V using machine model (C = 200pF, R = 0).
- Latch-up performance exceeds 500mA per JEDEC Standard JESD-17.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise.
- Flow-through architecture optimizes PCB layout.
- High-drive outputs (–32mA I_{OH}, 64mA I_{OL}).
- 74ABTH16260 incorporates bus-hold inputs which eliminate the need for external pull-up resistors.
- Package options:
  - 56-pin plastic Shrink Small-Outline Package (SSOP)
  - 56-pin plastic Thin Shrink Small-Outline Package (TSSOP)

DESCRIPTION

The 74ABT16260/74ABTH16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is alto useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ABTH incorporates the bus hold feature. The 74ABT does not include bus hold feature. Both parts are available in 56-pin SSOP and TSSOP.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx nBx to nAx	C_L = 50 pF	2.8 2.5	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0 V or 5.0 V	6	pF
I_{CCZ}	Total supply current	Outputs disabled	100	µA

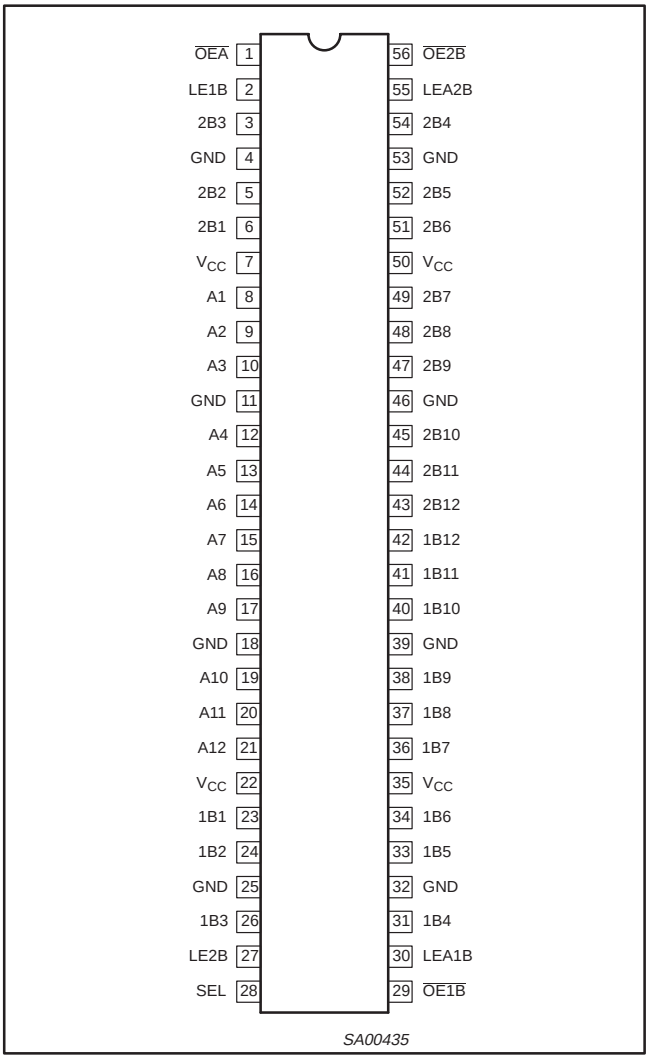
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16260 DL	BT16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16260 DGG	BT16260 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16260 DL	BH16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16260 DGG	BH16260 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21	An	Data inputs/outputs (A)
23, 24, 26, 31, 33, 34, 36, 37, 38, 40, 41, 42	1Bn	Data inputs/outputs (B1)
6, 5, 3, 54, 52, 51, 49, 48, 47, 45, 44, 43	2Bn	Data inputs/outputs (B2)
1, 29, 56	$\overline{OEA}$, $\overline{OE1B}$, $\overline{OE2B}$	Output enable input (active low)
2, 27, 30, 55	LE1B, LE2B, LEA1B, LEA2B	Latch enable inputs

PIN CONFIGURATION



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FUNCTION TABLES

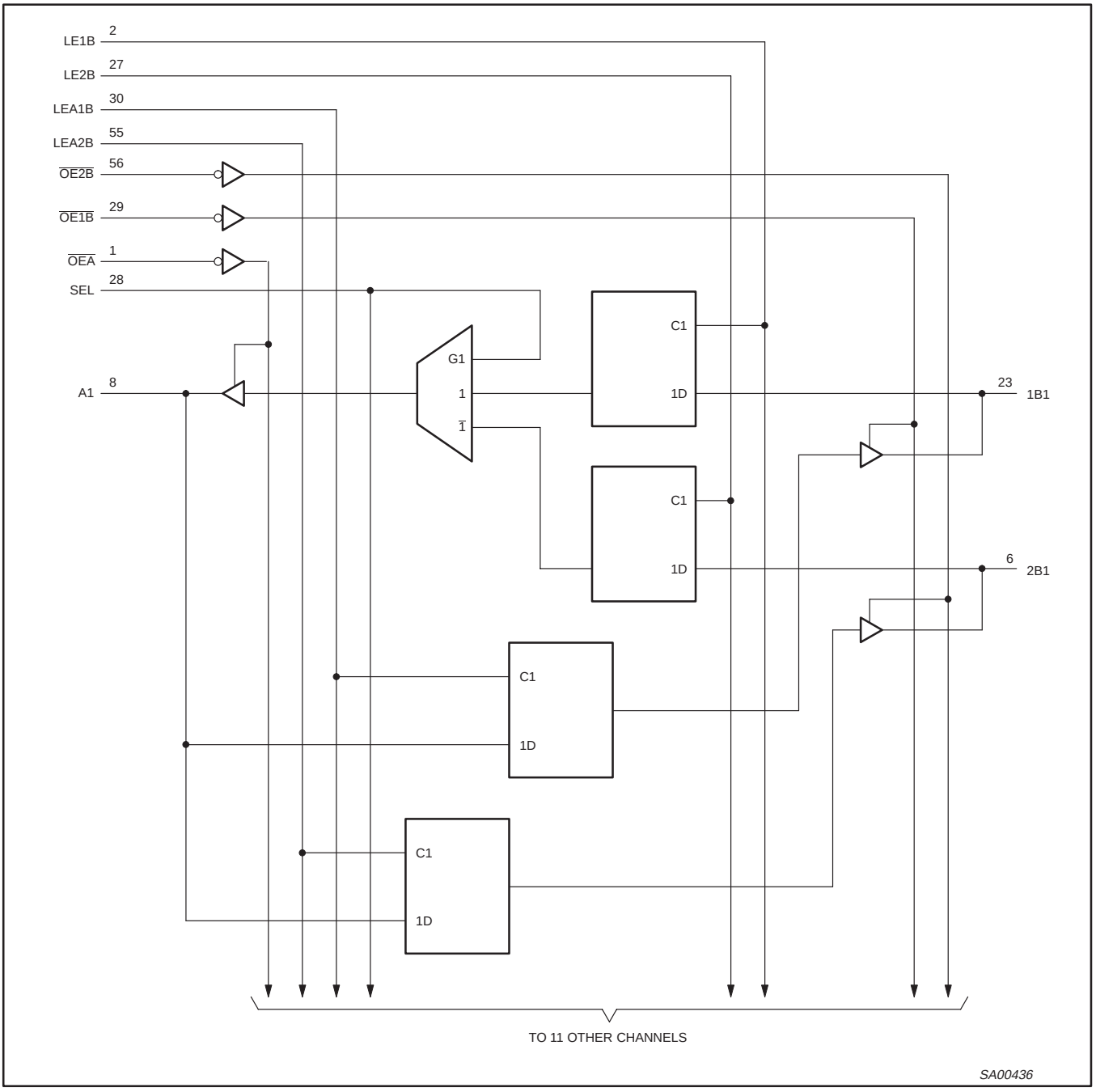
B to A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A0
X	X	X	X	X	H	Z

A to B ($\overline{OEA}$ = H)

INPUTS					OUTPUT	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B0
L	H	L	L	L	L	2B0
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L	L	L	L	1B0	2B0
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise specified)[1]

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range	see Note 2	–0.5	7	V
V_O	Voltage range applied to any output in the high state or power-off state		–0.5	5.5	V
I_O	Current into any output in the low state			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–18	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
	Maximum power dissipation at T_{amb} = 55°C (in still air)	see Note 3		1.4	W
T_{stg}	Storage temperature range		–65	+150	°C

NOTES:
1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER		LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t\Delta/v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t\Delta/V_{CC}$	Power-up ramp rate		200		µs/V
T_{amb}	Operating free-air temperature		–40	+85	°C

NOTE:
1. Unused or floating inputs must be held high or low.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.8	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC} or GND	Data pins			±3		±5	µA
I_{HOLD}	Bus Hold current	V_{CC} = 4.5V; V_I = 0.8V	A or B ports	75			75		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500			±500		
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = V_{CC}			±60	±200		±200	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}				50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–100	–225	–50	–225	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.2	1.5		1.5	mA
		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	
		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.1	1.0		1.0	
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			0.1	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
3. This is the bus hold minimum overdrive current required to force the input to the opposite logic state.

AC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		V_{CC} = 5V, T_{amb} = 25°C			T_{amb} = –40°C to +85°C		UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.8	4.8	1	5.6	ns
t_{PHL}			1	2.5	5	1	5.9	ns
t_{PLH}	$\overline{LE}$	A or B	1.1	3.2	4.9	1.1	5.8	ns
t_{PHL}			1.1	3.2	4.9	1.1	5.3	ns
t_{PLH}	SEL (B1)	A	1.3	3.2	4.6	1.3	5.3	ns
	SEL (B2)	A	1.1	2.8	4.9	1.1	6	ns
t_{PHL}	SEL (B1)	A	1.5	3.0	4.4	1.5	4.4	ns
	SEL (B2)	A	1.6	2.6	5.1	1.6	5.9	ns
t_{PZH}	$\overline{OE}$	A or B	1	2.9	4.7	1	5.7	ns
t_{PZL}			1.6	2.2	5.1	1.6	5.8	ns
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.1	5.4	2.2	6.4	ns
t_{PLZ}			1.3	3.2	4.4	1.3	4.8	ns

AC SETUP CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	V_{CC} = 5V, T_{amb} = 25°C		T_{amb} = –40°C to +85°C		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		1.5		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1		ns

AC WAVEFORMS

V_M = 1.5V for all waveforms
The outputs are measured one at a time with one transition per measurement.

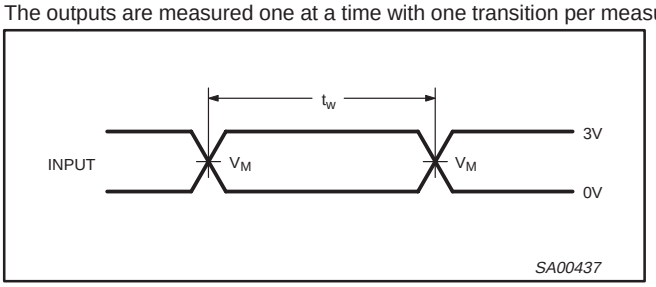


Figure 1. Pulse duration

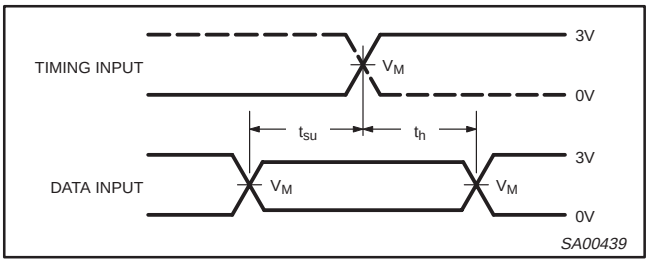
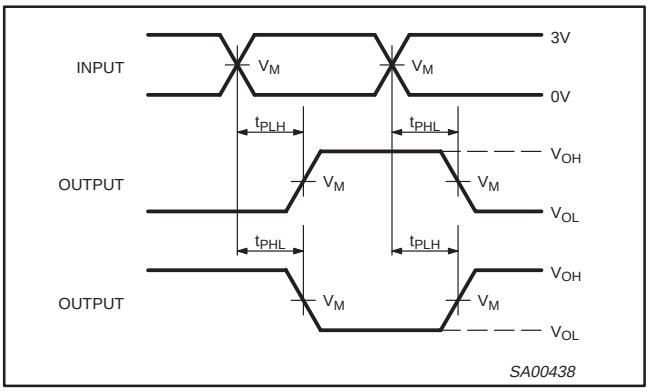
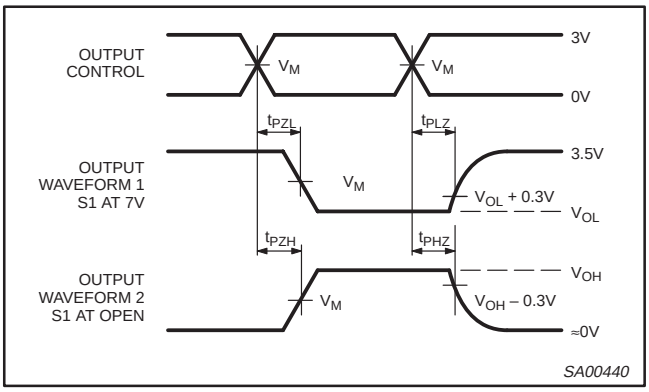


Figure 3. Setup and hold times



All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r ≤ 2.5ns, t_f ≤ 2.5ns.

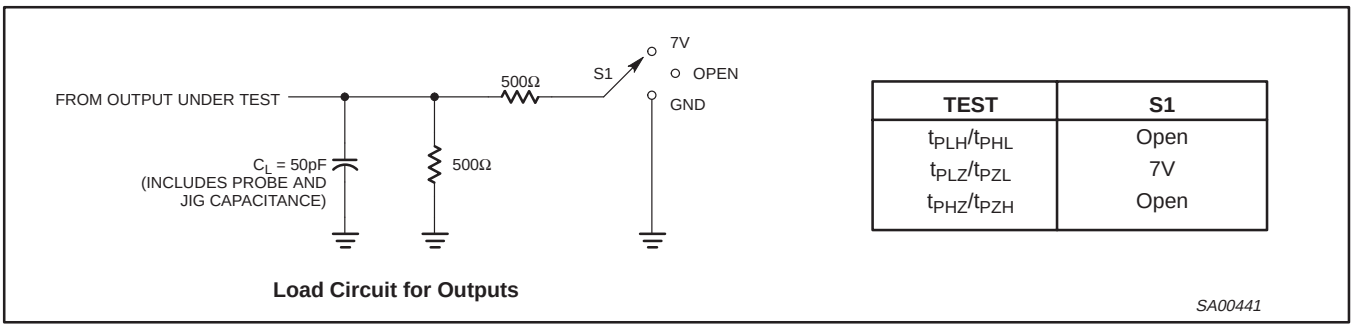
Figure 2. Propagation delay times; inverting and non-inverting outputs



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 4. Enable and disable times; low- and high-level enabling

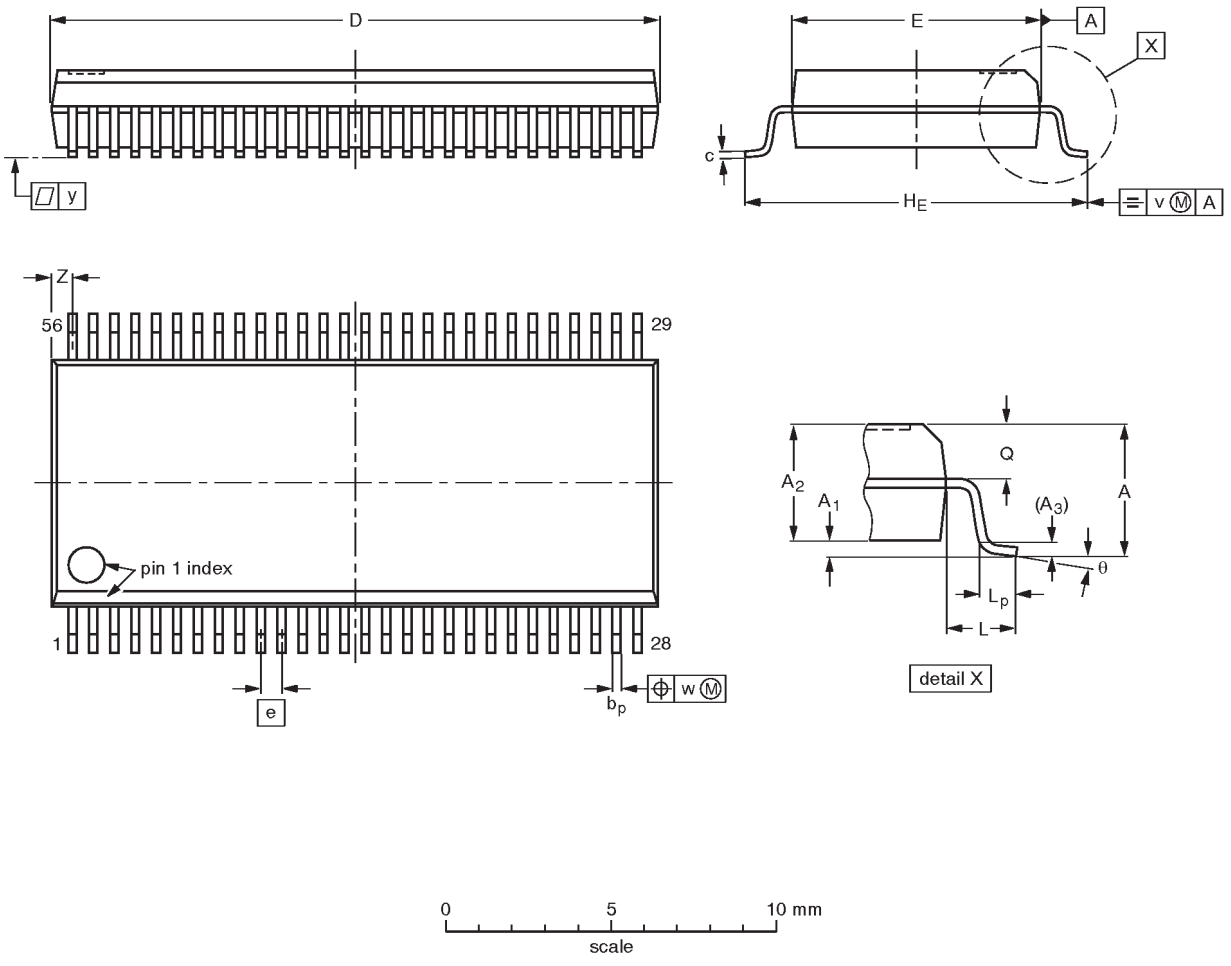
TEST LOAD CIRCUIT



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7V
t_{PHZ}/t_{PZH}	Open

Figure 5. Test load circuit

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

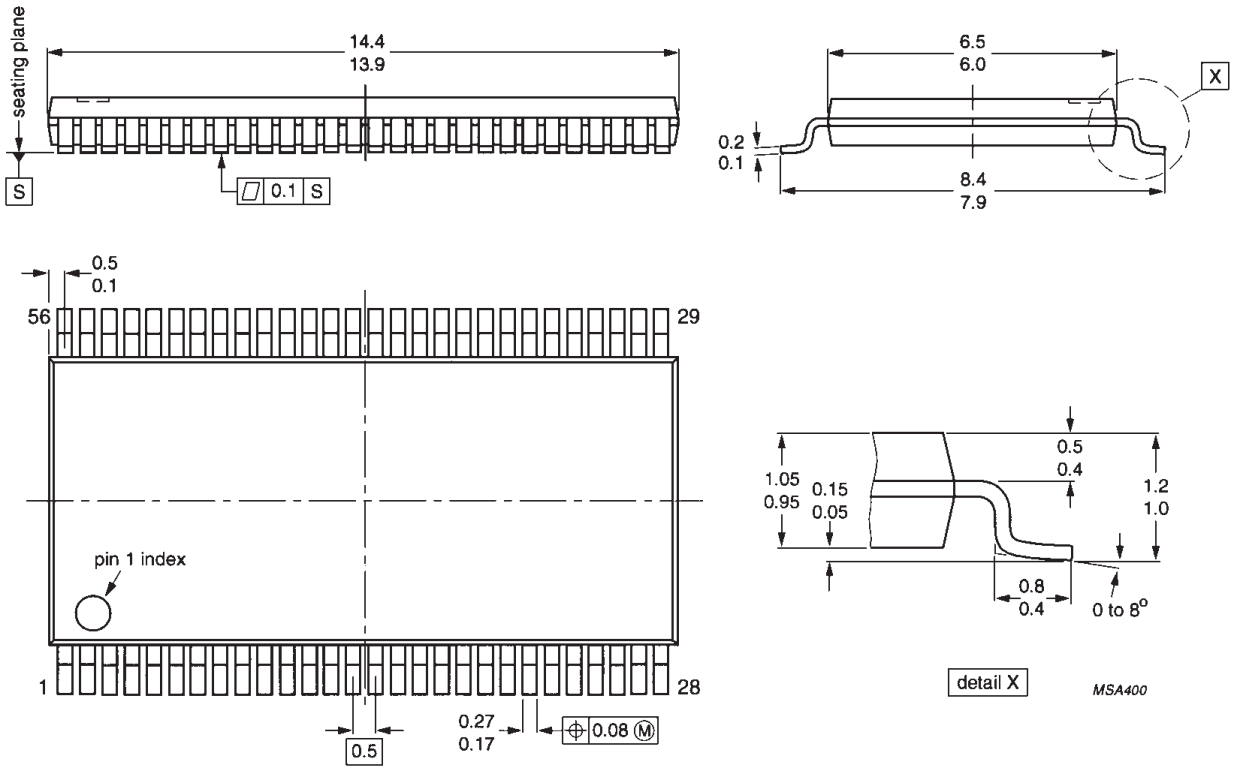
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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